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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,532	11/29/2001	Scott C. Glenn	42390P12946	5479

8791 7590 02/11/2004

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	8

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,532	GLENN, SCOTT C.	
	Examin r	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12/4/03

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1,3 and 23-26 is/are allowed.

6)☒ Claim(s) 6-8,10-22 and 27-34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 29 November 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED FINAL ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 10, 11, 16, 17, 27 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by No. 5,663,734 to Krasner.

In reference to Claim 10, Krasner discloses a system, comprising:

A first processor (Fig. 1A, element 26) having a first set of terminals for outbound data and a second set of terminals for inbound data (Fig. 1A, element 25, 33 and 35) and a register having a data field to determine the terminals in the first set that provide outbound data (inside microprocessor, Fig. 1A, element 26);

SRAM (Fig. 1A, element 30) coupled to the first processor; and

A second processor (Fig. 1A, element 32) having a first set of terminals for inbound data and coupled to the first set of terminals of the first processor (Fig. 1A, element 33), and a second set of terminals for outbound data and coupled to the second set of terminals of the first processor (Fig. 1A, element 33).

In reference to Claim 11, Krasner discloses a system of claim 10, further a register in the second processor having a data field to determine the terminals in the second set that provide outbound data (inside DSP, Fig. 1A, element 32).

In reference to Claims 16 and 17, Krasner discloses the system of claim 10, wherein the first processor is an applications processor (Fig. 1A, element 26) and the second processor is a baseband processor (Fig. 1A, element 32).

In reference to Claims 27 and 32, Krasner discloses a method and an article that comprise and result in:

transferring data from an application processor (Fig. 1A, element 32) to a baseband processor (Fig. 1A, element 26) through a first set of data pins (Fig. 1A, element 33); and

transferring data from the baseband processor to the applications processor through a second set of data pins (Fig. 1A, element 33).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-8 are rejected under 35 USC 103(a) as being unpatentable by Nakano in view of Krasner.

Nakano discloses a device, comprising: A storage register to store a data field value (Fig 1, element 14a); a channel to store data (Fig. 1, element 14b); and data terminals to provide data from the channel having a base value determined by the data field value (Fig. 1, element 14a). Nakano further discloses the device of claim 6 wherein hexadecimal and octal data is transferred from the channel storage (Fig. 1, element 14b) based on the value of the display register (Fig. 1,

element 14a). It is inherent that somewhere along the data path, at least four terminals are present for hexadecimal data, since hex requires a minimum of four binary digits to represent one hex number and four binary digits lines equate to four signal lines. The same argument applies for octal numbers. Select lines will be present to change between hex and octal base values (e.g., when either $12d_2$ or $12d_4$ is selected).

Nakano does not disclose expressly a terminal to provide a strobe signal, wherein an identity of a register to output data is provided at the data terminals during the strobe signal.

Krasner discloses a terminal to provide a strobe signal (Column 7, lines 0-8 refer to TMS320C30 and in the TMS320C30 spec, page 9, there is the primary and expansion bus interface strobes), wherein an identity of a register (e.g., the address for the registers/memory in the cache, page 12) to output data is provided at the data terminals during the strobe signal (the data terminals D0-D31, on page 3).

Nakano and Krasner are analogous art because they are from the same field of endeavor or similar problem solving area on current state of the art processors.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have strobe signals, whose purpose is to identify/trigger/sample for the data at particular address/register.

The suggestion/motivation for doing so would have been at a particular time, especially in synchronous systems, the user/processor needs to know the value of at a particular address.

Therefore, it would have been obvious to combine Nakano with Krasner for the benefit of strobe signals.

5. Claims 12-15, are rejected under 35 USC 103(a) as being unpatentable over Krasner in view of No. 5,901,074 to Nakano et al. (hereafter Nakano) in further view of Xilinx.

Krasner discloses the system of claim 10.

Krasner does not disclose expressly the system of claim 10 further comprising a channel in the first or second processor to supply or receive outbound or inbound data at the first or second set of terminals based on if it is hexadecimal or octal format specified by the data field.

Nakano discloses a system with the ability to select the data format, whether it is binary, octal or hexadecimal (Fig. 1, element 12).

Xilinx discloses an FPGA that can serve as a processor, with its pinout specified (Table 1). In particular, the clock out can be seen in Table 1 denoted as CCLK. Furthermore, eight data lines, which can be used to represent hexadecimal, octal, or binary number representations is seen in Table 1, denoted as D0-D7, capable of sending out octal or hexadecimal data through the respective data line terminals based a data field inside the processor.

Krasner, Nakano and Xilinx are analogous art because they are from the similar problem solving area in current implementations of processors.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the Xilinx FPGA to implement the processors described by Krasner with the selectable format by Nakano.

The suggestion/motivation for doing so would have been to use current programmable processor technology to implement DSP systems such as the one described by Krasner in addition to having a selectable number representation due to the availability of a plurality of data lines in the FPGA.

Therefore, it would have been obvious to combine Krasner, Nakano and Xilinx for the benefit of using current digital technology and selectable formats.

6. Claims 18-22 are rejected under 35 USC 103(a) as being unpatentable by Nakano in view of Krasner.

7. As per claims 18 and 19, Nakano discloses writing a data bit of a data field (Fig. 1, element 14); Storing data in a storage device (Fig. 1, element 14b); Providing the store data at data terminals in a first set of terminals (it is inherent terminals exist between Fig. 1, element 14 and element 11) and depending on the data being transferred, some terminal pins will not be active on both the transmit and receive side (Fig. 1, element 11 and 14).

Nakano does not disclose expressly a terminal to provide a strobe signal, wherein an identity of a register to output data is provided at the data terminals during the strobe signal.

Krasner discloses a terminal to provide a strobe signal (Column 7, lines 0-8 refer to TMS320C30 and in the TMS320C30 spec, page 9, there is the primary and expansion bus interface strobes), wherein an identity of a register (e.g., the address for the registers/memory in the cache, page 12) to output data is provided at the data terminals during the strobe signal (the data terminals D0-D31, on page 3).

Nakano and Krasner are analogous art because they are from the same field of endeavor or similar problem solving area on current state of the art processors.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have strobe signals, whose purpose is to identify/trigger/sample for the data at particular address/register.

The suggestion/motivation for doing so would have been at a particular time, especially in synchronous systems, the user/processor needs to know the value of at a particular address.

Therefore, it would have been obvious to combine Nakano with Krasner for the benefit of strobe signals.

8. As per claims 20-22, Nakano discloses claims 18, wherein hexadecimal and octal data is transferred followed by a strobe signal. It is inherent that somewhere along the data path, at least four terminals (or four consecutive signals, if coming from a serial transmittal view point) are present for hexadecimal data, since hex requires a minimum of four binary digits to represent one hex number and four binary digits lines equate to four signal lines. The same argument applies for octal numbers. Select lines will be present to change between hex and octal base values (e.g., when either $12d_2$ or $12d_4$ is selected). Furthermore, the data terminals will provide the address (hence the identification) of the storage device (e.g., the memory/cache in the device).

9. Claims 28-31, 33 and 34 are rejected under 35 USC 103(a) as being unpatentable over Krasner in view of Nakano in further view of Xilinx.

Krasner discloses a method and an article of Claims 27 and 32.

Krasner does not disclose expressly programming a register in the application or baseband processor to select data pins from the first set of data pins to provide hexadecimal, octal or binary data. Furthermore, Krasner does not disclose expressly transferring a clock signal from each processor to the other processor.

Nakano discloses a system with the ability to select the data format, whether it is binary, octal or hexadecimal (Fig. 1, element 12).

Xilinx discloses an FPGA that can serve as a processor, with its pinout specified (Table 1). In particular, the clock out can be seen in Table 1 denoted as CCLK. Furthermore, eight data lines, which can be used to represent hexadecimal, octal, or binary number representations is seen in Table 1, denoted as D0-D7.

Krasner, Nakano and Xilinx are analogous art because they are from the similar problem solving area in current implementations of processors.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to define the numbering system one desires for a digital system, in particular hexadecimal, octal or binary format as specified by Nakano. In the case of Xilinx, one can have two hexadecimal numbers, two octal numbers, or eight binary numbers at each clock cycle. Since there are three number representations to select from, at least two bits are required to select which data pins to group. It would be obvious to one of ordinary skill in the art to define these two bits in a register field due to the small storage space required.

The suggestion/motivation for doing so would have been to provide synchronous transfer of data between processors (for the case of sending a clock to and from processors) and defining the digital number representation to use by the processors.

Therefore, it would have been obvious to combine Krasner, Nakano and Xilinx for the benefit of synchronous data transfer and a selectable number representation.

Response to Arguments

10. Applicant's arguments, see page 10, first paragraph, filed 12/04/2004, with respect to Claims 1 and 6 have been fully considered and are persuasive. The 35 U.S.C §112 rejection of Claims 1 and 6 have been withdrawn.

11. As per 35 USC §102(b) rejection of claims 10, 11, 16, 17, 27 and 32, applicant's arguments consist of the following: "Krasner discloses only one set of terminals, i.e., bus 33, connects to processor 32 and microprocessor 26, and this set of terminals are I/O terminals. Thus, Krasner teachers I/O buffers having one common set of terminals to handle both inputs and outputs and not separate set of terminals as claimed in Applicant's claim 10. Second, Applicant claims a register having a data field to determine the terminals in the first set that provides outbound data" and "...Instead the bi-directional busses 33 and 35 are configured as either ALL inputs or ALL outputs. Although not shown in detail the direction of the I/O buffers are most likely based on a RW control signal, a signal that is not stored in a register as suggested by the Examiner" and " Krasner describes only one I/O bus, i.e., a bi-directional single set of terminals, an not separate first and second sets of terminals...".

Examiner wishes to point out that Krasner gives an example of the type of processor to be used in Column 7, lines 1-8, specifically TMS320C30 by Texas Instruments. Looking at the specification of the processor, it is evident that there is a dedicated data input line and a dedicated data output line. As an example, on page 3, the terminals/pins DR*n* and DX*n* are used just for data transmit output and data transmit receive (as defined on page 10 of the TMS320C30 specification). Further, there is a dedicated register (see page 12) for data-transmit and another for data-receive which are memory data fields that are directly at the terminal port of the processor where transmit and receive data go. Therefore, Krasner does anticipate a set of terminals for just input data and a set of terminals for just output data.

12. As per 35 USC §103(a) rejection of claims 12-15, applicant argues: "Krasner does not discloses a first processor having a first set of terminals for outbound data and a second set of

terminals for inbound data. Neither does Krasner disclose a second processor having a first set of terminals for inbound data that are coupled to the first set of terminals of the first processor, and a second set of terminals for outbound data that are coupled to the second set of terminals of the first processor."

Examiner wishes to point out again the TMS320C30. It is clear that if the TMS320C30 processor has a first set of terminals that only takes inputs and the second set of terminals that only takes outputs, the case is the same for the microprocessor that the TMS320C30, where it has a first set of terminals that takes outputs and a second set of terminals that takes inputs corresponding to the TMS320C30 processor terminals.

Allowable Subject Matter

13. 1,3 and 23-26 are allowed.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
02/4/2004

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